## EGC442 Class Notes 2/3/2023

Baback Izadi<br>Division of Engineering Programs<br>bai@engr.newpaltz.edu

```
/* This is a Verilog description for an 8 x 8
register file */
module regfile8x8
    (input write,
        input [2:0] wrAddr,
        input [7:0] wrData,
        input [2:0] rdAddrA,
        output reg [7:0] rdDataA,
        input [2:0] rdAddrB,
        output reg [7:0] rdDataB);
            reg [7:0] register [0:7];
            always @(*) begin
                case (rdAddrA)
            0: rdDataA = register[0];
            1: rdDataA = register[1];
            2: rdDataA = register[2];
            3: rdDataA = register[3];
            5: rdDataA = register[5];
            6: rdDataA = register[6];
            7: rdDataA = register[7];
            default: rdDataA = 8'hXX;
                endcase
    end
always @(*) begin
        case (rdAddrB)
    0: rdDataA = register[0];
```

1: rdDataA = register[1];
2: rdDataA = register[2];
3: rdDataA = register[3];
5: rdDataA = register[5];
6: rdDataA = register[6];
7: rdDataA = register[7];
default: rdDataA = 8'hXX;
endcase
end
always @(posedge write) begin
case (wrAddr)
0: register[0] <= wrData;
1: register[1] <= wrData;
2: register[2] <= wrData;
3: register[3] <= wrData;
4: register[4] <= wrData;
5: register[5] <= wrData;
6: register[6] <= wrData;
7: register[7] <= wrData;
endcase // case (wrAddr)
end // always @ (posedge write)
endmodule

## Instruction Count and CPI

Clock Cycles $=$ Instruction Count $\times$ Cycles per Instruction CPU Time $=$ Instruction Count $\times$ CPI $\times$ Clock Cycle Time

## $=\frac{\text { Instruction Count } \times \text { CPI }}{\text { Clock Rate }}$

- Instruction Count for a program
- Determined by program, ISA and compiler
- Average cycles per instruction
- Determined by CPU hardware
- If different instructions have different CPI
- Average CPI affected by instruction mix

5. Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time $f 250 \mathrm{ps}$ and a CPL of 2.0 for some program, and computer B has a clock cycle time of 500 ps and a CPI of 1.2 for the same program.

$$
\begin{aligned}
& T_{A}=250 \times 10^{-12} \mathrm{sec} \rightarrow 4 \mathrm{G} 1 \mathrm{c}-10 \\
& T_{B}=\overline{50 g} \times 10^{-12^{\prime \prime}} \rightarrow \frac{10^{10}}{5}=2 \mathrm{G}(1)
\end{aligned}
$$

a. How does one know that each computer executes the same number of instructions for the program? All computers use the same number of instructions for a given program.
$\checkmark$ Both computers use the same instruction set architecture.
Both computers use the same implementation.
b. Which computer has a faster clock? Computer A
Computer B

$$
t E X_{Q}=\# \text { of ins }
$$

c. Which computer requires fewer clock cycles to execute a single instruction?

d. If Computer A executes 1000 instructions for the program, what is the program's CPU time on Computer A?
$1000 \mathrm{instr}^{*} 2.0$ cycle $/ \mathrm{instr} * 250 \mathrm{ps} /$ cycle $=500,000 \mathrm{ps} \rightarrow$ TQ Ked. A
$1000 \mathrm{instr} * 1.2$ cycle $/ \mathrm{instr} * 500 \mathrm{ps} /$ cycle $=600,000 \mathrm{ps} . \rightarrow$ Tepee $\beta$
e. If Computer A executes 1000 instructions for the program, how many instructions does Computer B execute for the program?

```
1000
```

$1000 * 1.2=1200$
$1000 * 2.0=2000$
f. For a particular program, Computers A and B execute 2000 instructions. A's CPU time is 2000 * 20 * $250=1,000,000 \mathrm{ps}$. Bs is $2000 * 1.2 * 500=1,200,000 \mathrm{ps}$. How much faster is Computer A than B?

h. Computer A is better than Computer B .

7. Computer C's performance is 4 times as fast as the performance of computer B , which runs a given application in 28 seconds. How long will computer C take to run that application?

$$
\frac{28}{4}=7 \mathrm{sec} .
$$

$$
t_{C}=\frac{t_{B}}{4} \Rightarrow 28
$$

(6)


$$
\text { He le = } 2 \times 1 \times 1 \times 1 \times 2 \times 3 \text {. }
$$

cyl el

$$
\text { b. Codes sequencer executes } 6^{\text {obstructions. }} 1 / 6=1.5
$$

Code sequence 2 requires $q$ CPU clock cycles.
Assume a new code sequence 3 contains the following ins
${ }_{c}^{\text {code }} \rightarrow 5$ ins instruction class. What is code sequence 3's CPU clock cycles?

$$
\rightarrow 36
$$

$$
\text { Cit of } \overrightarrow{\text { ins }}=10+4+6=20
$$

$$
C P I=\frac{36}{20}=1.8
$$

For a given number of instructions, assume CPI is increased by $20 \%$, and clock

$$
\begin{aligned}
& \text { exec }=\# \text { of inst } * C P \pm * T C y c \\
& \text { 200\% } 10 \% \\
& T_{\text {Tenet new }}=\text { trabinst*CPI*1.2*Tengc* } 0.9 \\
& =1.08 * \& \text { inst } * C P \text { * } T_{\text {by }}
\end{aligned}
$$

Increases
slower system
4. Our favorite program runs in 10 seconds on computer A, which has a 2 GHz clock. We are trying to help a computer ser build a computer, B, which will run this program in 6 seconds. The designer has determined that a substantial ..cease in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer B to req


$$
\begin{aligned}
& \text { b. Computer B's performance is improved by reducing the } \\
& \text { Tench }=\text { Instr *CPI*T } T_{B} / \frac{10}{6}=\frac{1}{1.2} * \frac{.5}{T} f
\end{aligned}
$$

$$
\begin{aligned}
& \text { Terence } B=\overline{G \sec }=\operatorname{ins} A_{r} \times 1.2 c P A_{1} * \bar{C}_{B} \rightarrow T_{B}=\frac{5 n 5 \times 6}{10_{2} \times 1 / 2}
\end{aligned}
$$

7. Assume CPI and clock cycle time remain constant. Reducing the instruction count will reduce the program's execution time.

$$
\text { tenrec }=\text { \#of Instr } / * C P I * \text { clock period }
$$

yes

2 A clock rate of 1 GHz corresponds to a period of 1 nanosecond, which is $1 \times 109$ seconds.

$$
G_{1 \times 10^{9}}
$$

$$
V_{T}=\frac{1}{1 \times 10^{10}}=1 \times 10^{-9}
$$

